respectfully requests that the rejection under 35 U.S.C. § 103(a) be withdrawn for the following reasons.

Burlison describes a method and apparatus for determining the quiescent power supply current of a device under test. *Burlison* achieves this objective by detecting the slope of the time rate of change in voltage for a node. More specifically, the apparatus compares voltages measured before and after decoupling a power supply from the node. *See* col. 3, ll. 65-67 and col. 4, ll. 1-5.

Schinabeck describes a method and apparatus for applying analog voltages or currents to nodes of a device under test. Further, *Schinabeck* describes monitoring resulting currents or voltages with the purpose of evaluating electrical characteristics of the device under the test. According to *Schinabeck,* the described method and apparatus increase test rates by reducing the impact of analog settling time. *See* col. 3, ll. 22-29.

Claim 1 is directed to a semiconductor testing apparatus comprising a combination of elements including, *inter alia*, "a decision circuit for comparing current-value change rates obtained by supplying the plurality of test vectors to faulty samples with the range of pass/fail decision criteria per address pair, and for deciding whether the target test device is a good sample as a non-defective semiconductor device or a faulty sample based on the current-value change rates corresponding to the address pairs extracted based on the comparison results obtained." Neither *Schinabeck* nor *Burlison*, however, teaches or suggests the claimed combination including, at least,

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deciding whether the target test device is a good sample as a non-defective semiconductor device or a faulty sample based on the current-value change rates corresponding to the address pairs extracted based on the comparison results obtained.

Moreover, *Burlison* teaches away from this feature of claim 1 by pointing out that the monitor circuit 400 (Fig. 5) detects whether the voltage at the node increases or decreases over the time instead of measuring the change in voltage. *See* col. 5, ll. 4-15. *Schinabeck* does not overcome this deficiency. Finally, neither *Schinabeck* nor *Burlison* provides motivation to combine their teachings and the Examiner has identified none. Therefore, claim 1 is patentable over *Schinabeck* and *Burlison*.

Claims 2 – 4 depend from claim 1 and include all the elements thereof and are allowable at least based on such dependency.

Claim 5 is directed to a semiconductor testing method comprising a combination of elements including, *inter alia*, "calculating a current-value change rate per address pair forming two different addresses, and outputting this current-value change rate as the current-value change rate of the good sample."

Neither *Schinabeck* nor *Burlison*, however, teaches or suggests the claimed combination including, at least, calculating a current-value change rate per address pair forming two different addresses, and outputting this current-value change rate as the current-value change rate of the good sample. To the contrary, instead of measuring the change in voltage, *Burlison* teaches comparing voltages for two subsequent testing of the device with the purpose of determining whether voltage increased or decreased

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over time. See col. 6, ll. 42-48. According to *Burlison,* "[a] passing part has a voltage V_{DUT} that increases over time, wherein a failing part has a voltage that decreases over time." *See* id. In other words, nowhere does *Shinabeck* or *Burlison* teach outputting a "current-value change rate as the current-value change rate of the good sample." *Schinabeck* does not overcome this deficiency. Therefore, claim 5 is patentable over *Shinabeck* and *Burlison*.

Claims 6 – 8 depend on claim 5 and include all the elements thereof and are allowable at least based on such dependency.

Claim 9 is directed to a program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus comprising a combination of procedures including "calculating a current-value change rate between two current values corresponding to an address pair forming two different addresses, and outputting the calculated current-value change rates as the current-value change rates of the good samples."

Again, as discussed above with respect to claim 5, neither *Schinabeck* nor *Burlison* teaches or suggests the claimed combination including, at least, forming two different addresses, and outputting the calculated current-value change rates as the current-value change rates of the good samples. Furthermore, *Burlison* teaches away from this feature of claim 9 by pointing out that the monitor circuit 400 (Fig. 5) detects whether the voltage at the node increases or decreases over the time instead of

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measuring the change in voltage. *See* col. 5, ll. 4-15. *Schinabeck* does not overcome this deficiency. Therefore, claim 9 is patentable over *Schinabeck* and *Burlison*.

Claims 10 – 12 depend from claim 9 and include all the elements thereof and are allowable at least based on such dependency.

Claim 13 is directed to a semiconductor testing method of specifying a faulty part in a semiconductor product comprising a combination of steps including "supplying a plurality of test vectors to good and faulty samples as semiconductor devices, and measuring current values corresponding to addresses indicating the test vectors; calculating current-value change rates between current values corresponding to an address pair consisting of two addresses in each of the good and faulty sample; and comparing the current-value change rates corresponding to the address pairs in each of the good and faulty samples, and determining address pairs of the test vectors to be used for performing an emission analysis that is useful to specify a faulty part in a semiconductor device."

Neither *Schinabeck* nor *Burlison*, however, teaches or suggests the claimed combination including, at least, calculating current-value change rates between current values corresponding to an address pair consisting of two addresses in each of the good and faulty sample. Moreover, *Burlison* teaches away from this feature of the current invention by pointing out that the need for quantitative analysis of the voltage is obviated. According to *Burlison,* monitor 400 (Fig. 5) detects only the slope polarity of

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the time rate of change. *Schinabeck* does not overcome this deficiency. See col. 5, ll. 5-15. Therefore, claim 13 is patentable over *Schinbeck* and *Burlison*.

Claims 14 – 18 depend from claim 13 and include all the elements thereof and are allowable at least based on such dependency.

Finally, claim 19 is directed to a semiconductor testing apparatus for specifying a faulty part in a semiconductor device comprising a combination including, *inter alia*, "a current-value change rate calculation circuit for calculating a current-value change rate per test vector pair in each of the good and faulty samples, the number of the test vector pairs being a desired number, by using the current values from the current-value measuring circuit."

Neither *Schinabeck* nor *Burlison*, however, teaches or suggests a combination including, at least, calculating a current-value change rate per test vector pair in each of the good and faulty samples. As discussed above with respect to claims 5, 9, and 13, *Burlison* teaches away from this feature of the current invention, and *Schinabeck* does not overcome this deficiency. Therefore, claim 19 is patentable over *Schinabeck* and *Burlison*.

In view of the foregoing amendments and remarks, Applicant respectfully requests the reconsideration and reexamination of this application and the timely allowance of the pending claims.

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Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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Dated: August 9, 2002

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